Effective Post-Programming Screening of Antifuse FPGAs for Space Applications

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Abstract

For a decade, HIREC has been working for post-programming screening of antifuse FPGAs and supplying the FPGAs to Japanese space customers, meeting with the full technical satisfactions.

In this paper, we report the results on the effectiveness of the post-programming screening for antifuse FPGAs to ensure the reliable use of the FPGAs.
Introduction of HIREC

HIREC

is a test house
qualified by JAXA (Japan Aerospace Exploration Agency)

• quality assurance (surveillance, source inspection, etc.)
• screening and quality conformance inspection
• environmental test (radiation test, etc.)
• Destructive physical analysis, construction analysis
  and failure analysis (SEM inspection, etc.)
for semiconductor devices (MPU, Gate Array, Memory, etc.)
for space applications.

performs design of semiconductor devices
for space application.

• design (MPU, Memory, FPGA, etc.)
1. Purpose of post-programming screening

(1) Post-Programming Electrical Parameter Test (PPEPT)
To ensure the electrical parameters as a built configuration.

Because:
- Actual delay parameters cannot be measured for blank devices.
- Programming instruments doesn’t assure the electrical performance (i.e. functionality, timing, and so forth) in full operating range.

PPEPT is necessary for programmed antifuse FPGAs.

(2) Post-Programming Dynamic Burn-In (PPDBI)
To screen the potential damage to internal logic elements during device programming.

Because:
- High programming voltage (Vpp) may damage the internal logic elements.
- Dynamic burn-in is the most effective way to exercise all the active elements as a built configuration.

PPDBI is necessary for programmed antifuse FPGAs.
## HIREC Post-programming screening flow

<table>
<thead>
<tr>
<th>HIREC Class I Flow</th>
<th>HIREC Class II Flow</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pre Burn-In Electrical Parameters Test at +25°C</strong> (1)(2)</td>
<td>Pre Burn-In Electrical Parameters Test at +25°C (1)</td>
</tr>
<tr>
<td>Dynamic Burn In +125°C, 240hrs</td>
<td>Dynamic Burn-In +125°C, 160hrs.</td>
</tr>
<tr>
<td>Interim (Post Burn-In) Electrical Parameters Test at +25°C (2)(4)</td>
<td>N/A</td>
</tr>
<tr>
<td>Delta Calculation, Percent Defective Allowable (PDA) (3)(4)</td>
<td>N/A</td>
</tr>
<tr>
<td>Static Burn-In at +150°C, 72hrs (4)</td>
<td>N/A</td>
</tr>
<tr>
<td>Final Electrical Parameters Test at +25°C (2)</td>
<td>Final Electrical Parameters Test at +25°C (2)</td>
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<tr>
<td>Delta Calculation, Percent Defective Allowable (PDA) (3)</td>
<td>Delta Calculation, Percent Defective Allowable (PDA) (3)</td>
</tr>
<tr>
<td>Final Electrical Parameters Test at -55°C, +125°C (2)</td>
<td>Final Electrical Parameters Test at -55°C, +125°C (2)</td>
</tr>
<tr>
<td>External Visual</td>
<td>External Visual</td>
</tr>
</tbody>
</table>

Notes: (1) Pre Burn-In electrical parameters tests are measured for Subgroup 1, 7, and 9.
(2) Interim (Final) electrical parameters tests are measured for Subgroup 1, 7 and 9 (1, 2, 3, 7, 8, 9 and 10) listed on MIL-PRF-38535, Table III.
(3) Delta calculation is performed for the parameters specified in SMD.
(4) Option.
Electrical parameters test system in HIREC

LSI test system

Dynamic burn-in test system in HIREC

Full dynamic burn-in system

An example of DUT board

An example of burn-in board
## 2. Results of post-programming screening

### Post-programming screening summary performed in HIREC

<table>
<thead>
<tr>
<th>Product</th>
<th>Package</th>
<th>IN</th>
<th>OUT</th>
<th>Test Item/Number of Failures or Issues</th>
<th>Pre Burn-In PPEPT</th>
<th>PPDBI</th>
<th>Final PPEPT (at +25°C)</th>
<th>Delta Calculation</th>
<th>Final PPEPT 125°C</th>
<th>Final PPEPT -55°C</th>
<th>Others Issues of electrical parameters</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(1)</td>
<td>(2)</td>
<td>(3)</td>
<td>(4)</td>
<td>(5)</td>
<td>(6)</td>
<td>(7)</td>
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<td>1 4 3 4 1 0 3 2 1</td>
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</tbody>
</table>

Note: The numbers from (1) to (7) are related to those of following presentation.

(a)~(e) means fail mode on electrical parameters as shown below;
(a)•••Standby supply current (IDD(STB))
(b)•••Input leakage current (IIL/IIH)
(c)•••Functional Test (FT) (“Functionality” only for PPDBI)
(d)•••Output voltage (VOL/VOH)
(e)•••All parameters
2. Results of post-programming screening (cont.)

(1) Programming

- Programming
  - Total: 3019 pcs.

- Failure
  - Total: 100 pcs.

Summary of programming performed in HIREC

(2) Pre burn-in electrical parameters test at 25°C by LSI tester.

- Standby supply current (IDD(STB))
  - RP1280A (1pc.)
  - RT14100A (1pc.)
  - RT54SX32 (1pc.)
  - RT54SX32S (3pcs.)

- Input leakage current (IIL/IIH)
  - A1280A (1pc.)
  - RP1280A (1pc.)
  - RH1280 (1pc.)

- Functional test (FT)
  - A1280A (1pc.)
  - RT14100A (1pc.)
  - RT54SX32 (1pc.)

Note: There are 2 designs whose number of failures exceeded the maximum number of allowed programming failures defined by the manufacturer.

- The instruments cannot ensure the quality/reliability of programmed FPGAs.
Anomalous delta for IDD(STB) for the same designed **RT54SX16** (4pcs. from 4pcs.)

(3) Post-Programming Dynamic Burn-In (PPDBI)

Anomaly of Functionality and Operating current during burn-in

**A1280A** (1pc.)

**RH1280** (1pc.)

(4) Final electrical parameters test at 25 °C

Standby supply current

**RT54SX16** (1pc.)

Catastrophic damage

**A1280A** (1pc.)

(5) Delta calculation

Standby supply current

**RT54SX16** (3pcs.)

**RH1280** (1pc.)

Anomalous delta for IDD(STB) for the same designed **RH1280** (1pcs. from 4pcs.)

Spec limit: 25mA

Spec limit: ± 2.5mA
(6) Final electrical parameters test at -55 and +125°C

Input leakage current (IIL/IIH)

- RT54SX16 (1pc.)

Functional test (FT)

- RT14100A (3pcs.)

Output voltage (VOH)

- RT54SX16 (4pcs.)

All parameters

- RP1280A (1pc.)

S/N 2061 failed the input leakage current (IIL/IIH) at +125°C for the same designed RP1280A

<table>
<thead>
<tr>
<th>S/N</th>
<th>Pin No.</th>
<th>IIL [μA]</th>
<th>IIH [μA]</th>
<th>Ta (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>-55</td>
<td>+25</td>
<td>+125</td>
</tr>
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</tr>
</tbody>
</table>

Notes:
(1) OVER means range over in measurement.
(2) Max Limits: ±10[μ A]
4. Conclusion

The post-programming screening has revealed that some portion of the antifuse FPGAs were defective after programming.

The schedule and costs might be strongly affected, if the above problems are discovered on the FPGAs embedded in the flight hardware.

The post-programming screening for antifuse FPGAs is mandatory for space applications.